

CLAIMS

1. A circuit arrangement comprising:

a multi-mode bias circuit comprising a control voltage input, a mode control input for selecting between a linear mode and a saturation mode, and a bias output;

5 an amplifier comprising a bias input connected to said bias output of said multi-mode bias circuit, said amplifier further comprising an RF input and an RF output; said multi-mode bias circuit causing an RF output power at said RF output to be proportional to an RF input power at said RF input when said mode control input selects said linear mode;

10 said multi-mode bias circuit causing an RF output power at said RF output to be determined by said control voltage input when said mode control input selects said saturation mode.

2. The circuit arrangement of claim 1 wherein said mode control input is

15 coupled to a controlled current source for enabling said controlled current source in said linear mode and for disabling said controlled current source in said saturation mode.

3. The circuit arrangement of claim 1 wherein mode control input is coupled to a switch, said switch enabling a path between said control voltage input and said bias 20 output of said multi-mode bias circuit in said saturation mode, said switch disabling a path between said control voltage input and said bias output of said multi-mode bias circuit in said linear mode.

4. The circuit arrangement of claim 3 wherein said path comprises a transistor situated between said switch and said bias output of said multi-mode bias circuit.

5 5. The circuit arrangement of claim 4 wherein said transistor is a FET configured as a voltage follower transistor, wherein a gate of said FET is coupled to said switch and a source of said FET is coupled to said bias output of said multi-mode bias circuit.

10 6. The circuit arrangement of claim 1 wherein said multi-mode bias circuit comprises a controlled current source coupled between VDD and a gate of a FET, said gate of said FET being coupled to a switch, said switch being coupled to said control voltage input, a drain of said FET being coupled to VDD, a source of said FET being said bias output of said multi-mode bias circuit.

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7. The circuit arrangement of claim 6 wherein said multi-mode bias circuit further comprises a bipolar transistor having a collector coupled to said gate of said FET, an emitter coupled to ground, and a base coupled to said source of said FET.

20 8. The circuit arrangement of claim 6 wherein said mode control input is coupled to said controlled current source for enabling said controlled current source in said linear mode and for disabling said controlled current source in said saturation mode.

9. The circuit arrangement of claim 6 wherein mode control input is coupled to said switch, said mode control input closing said switch in said saturation mode, said mode control input opening said switch in said linear mode.

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10. The circuit arrangement of claim 6 further comprising a resistor between said control voltage input and said switch.

11. A circuit comprising:

10 a biasing means for causing an amplifier to operate in a linear mode or a saturation mode;

    said biasing means comprising a controlled current source, said controlled current source being enabled in said linear mode and being disabled in said saturation mode;

15     said biasing means further comprising a switch coupled to a control voltage input, said switch being closed in said saturation mode and being open in said linear mode.

12. The circuit of claim 11 wherein a mode control input selects between said linear mode and said saturation mode.

20     13. The circuit of claim 12 wherein said mode control input enables said controlled current source in said linear mode and disables said controlled current source in said saturation mode.

14. The circuit of claim 12 wherein said mode control input closes said switch in said saturation mode and opens said switch in said linear mode.

5 15. The circuit of claim 11 wherein a bias output of said biasing means is connected to a bias input of said amplifier.

16. A circuit comprising:

a biasing means for causing an amplifier to operate in a linear mode or a saturation mode;

said biasing means comprising a controlled current source, said controlled current source coupled to a gate of a transistor, said controlled current source being enabled in said linear mode;

15 said biasing means further comprising a control voltage input, said control voltage input coupled to said gate of said transistor in said saturation mode;

wherein a source of said transistor is a bias output of said biasing means.

17. The circuit of claim 16 wherein a mode control input selects between said linear mode and said saturation mode.

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18. The circuit of claim 17 wherein said mode control input is coupled to said controlled current source so as to enable said current source in said linear mode and to

disable said controlled current source in said saturation mode.

19. The circuit of claim 17 wherein said biasing means further comprises a switch between said control voltage input and said gate of said transistor, wherein said 5 mode control input is coupled to said switch, said mode control input closing said switch in said saturation mode and opening said switch in said linear mode.

20. The circuit of claim 19 further comprising a resistor between said switch and said control voltage input.